Notice of Allowability	Application No.	Applicant(s)	
	10/606,283	SHINOMIYA, NORIKO	
	Examiner	Art Unit	
	Nghia M. Doan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Application filed on 06/23/2003 and RCE for IDS filed on 04/05/2006*.

2. ☒ The allowed claim(s) is/are *1-4, 9-12, 18, and 22, renumbered (37 CFR 1.126)*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 11/29/05; 02/22/06; and 04/05/2006.
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

JACK CHIANG
SUPERVISORY PATENT EXAMINER

DETAILED ACTION

1. Responsive to communication application 10/606,283 filed on 10/24/2005 and Request for Continued Examination filed on 04/05/2006, claims 1-4, 9-12, 18, and 22 are pending.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 11/29/20005; 02/22/2006; and 04/05/2006 are being considered by the examiner.

Allowable Subject Matter

3. Claims 1-4, 9-12, 18, and 22 allowed.

The following is an examiner's statement of reasons for allowance: taking claim 1 as exemplary, the prior art made of records does not teach or fairly suggest in the combination of the inventive steps comprising: an input means for inputting gate level logic circuit information, standard cell library information, and package information of a circuit block as a constituent of the semiconductor integrated circuit; a noise analysts means for performing noise analysis for the circuit block using the information inputted by the input means; a noise judgement means for judging whether the amount of noise that occurs in the circuit block is within a predetermined range or not, on the basis of a result of noise analysis by the noise analysis means; a processing ending means for ending the automatic generation of the pattern of the semiconductor integrated circuit, when it judged by the noise judgement means that the amount of noise is within the predetermined range; logic gate selection means for selecting a logic gate in the circuit block, which logic gate generates an amount of noise larger than a predetermined

amount of noise, When it is judged by the noise judgment means that the amount of noise in the circuit block is out of the predetermined range; and a bypass condenser addition means for adding a bypass condenser for reducing power supply noise and substrate noise to the selected logic gate".

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Remarks

4. Yano Junichi (Japanese Publication Number: 2002-9158, Publication date 11/01/2202) is the closest prior art to disclose a method for analyzing and reducing noise that is directly to a standard cell, which is stored in the library for an integrated circuit, but Yano Junichi does not teach or suggest that when the circuit block noise is out of a predetermine range then a logic gate is selected in the circuit block, which the logic gate generates an amount of noise larger than a predetermined amount of noise and adding a bypass condenser (capacitance) for reducing the power supply noise and substrate noise to the selected gated.

5. Hiroshi Wabuka (EP 1143507 A1) is also the closest prior art to disclose a method to analysis and reduction an EMI noise in the integrated circuit using a bypass capacitance incorporated into logic gate to reduce EMI noise generated in an IC, But Hiroshi Wabuka at least does not teach selecting a logic gate in the circuit block, which the logic gate generates an amount of noise larger than a predetermined amount of

noise and adding a bypass condenser (capacitance) for reducing the power supply noise and substrate noise to the selected gated.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nghia M. Doan
Patent Examiner
AU 2825
NMD

JACK CHIANG
SUPERVISORY PATENT EXAMINER